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आई आई टी हैदराबाद
IIT Hyderabad

Chips to Startup Programme
An initiative by Ministry of Electronic and IT, Government of India

SYNOPSYS®
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VLSI System Design

# Cloud based Analog IC Design Hackathon

This is to certify that

*Vinod Kumar Yadav*

from

*Government Girls Polytechnic Gorakhpur*

has designed the circuit

*Non-overlapping clock generator for micro scale energy harvesting applications in 28nm CMOS technology*

using Synopsys Custom Compiler Platform

She/He has performed an ~~Outstanding~~/**Excellent**/~~Very Good/ Good~~ work.

**This program was conducted between 15 February - 1 March 2022 as an initiative of IIT Hyderabad, which has been sponsored by Synopsys in association with VLSI System Design (VSD) Pvt.**

**Dr Ashudeb Dutta**
Program Co-Ordinator, IIT Hyderabad

**Dr B Umashankar**
Chair CCE, IIT Hyderabad

This is computer generated certificate. To verify visit https://hackathoniith.in