







## Cloud based Analog IC Design Hackathon

This is to certify that

Vignesh Bharadwaj

Birla Institute of Technology and Science, Pilani, Hyderabad Campus

has designed the circuit

Approximate Compressor for error-resilient Multiplications

using Synopsys Custom Compiler Platform
She/He has performed an Outstanding/Excellent/Very Good/Good-work.

This program was conducted between 15 February - 1 March 2022 as an initiative of IIT Hyderabad, which has been sponsored by Synopsys in association with VLSI System Design (VSD) Pvt.

**Dr Ashudeb Dutta** 

Program Co-Ordinator, IIT Hyderabad

**Dr B Umashankar** Chair CCE, IIT Hyderabad

Jecemeshanker