







Cloud based Analog IC Design Hackathon

This is to certify that

P Santosh Kumar Patra

Analog Devices

has designed the circuit

Design of a low power 8×8 hybrid Dadda-Vedic multiplier

using Synopsys Custom Compiler Platform
She/He has performed an Outstanding/Excellent/Very Good/Good work.

This program was conducted between 15 February - 1 March 2022 as an initiative of IIT Hyderabad, which has been sponsored by Synopsys in association with VLSI System Design (VSD) Pvt.

Dr Ashudeb Dutta

Program Co-Ordinator, IIT Hyderabad

Dr B Umashankar Chair CCE, IIT Hyderabad

Jecemeshanker